What is claimed is:

1. An integrated circuit comprising:

bus request logic configured to assert a bus request signal;

functional logic operative to control transactions over a system bus as a bus master, after receiving a bus grant signal; and

clock control logic configured to disable at least one clock signal used to clock synchronous circuitry of the functional logic in response to the assertion of bus request signal, the clock control logic further configured to enable the at least one clock signal in response to receipt of the bus grant signal.

2. The integrated circuit of claim 1, further comprising functional logic that operates in a synchronous manner in response to the at least one clock signal.

3. An integrated circuit comprising clock control logic configured to disable at least one clock signal of the integrated circuit in response to a bus request signal, the clock control logic further configured to enable the at least one clock signal in response to receipt of a bus grant signal.

4. An integrated circuit capable of being a bus master, the improvement comprising clock control logic capable of disabling or inhibiting a clock signal of the integrated circuit after assertion by the integrated circuit of a bus request signal, the clock control logic further capable of enabling the clock signal substantially commensurate with receipt of a bus grant signal.

5. The integrated circuit of claim 4, further comprising synchronous logic that operates in response to the clock signal.

6. An integrated circuit capable of being a bus master comprising clock control logic configured to disable at least one clock signal of the integrated circuit during a period of time between a first time in which the integrated circuit has requested to be a bus master and a second time in which bus mastership has been assumed by the integrated circuit.

7. The integrated circuit of claim 6, wherein the clock control logic is more specifically configured to disable the at least one clock signal during substantially the entire period of time in which the integrated circuit has requested to be a bus master and the time when bus mastership has been assumed by the integrated circuit.

8. The integrated circuit of claim 6, wherein the clock control logic comprises circuitry configured to disable the at least one clock signal in response to a bus request signal.

9. The integrated circuit of claim 6, wherein the clock control logic comprises circuitry configured to disable the at least one clock signal substantially commensurate with a bus request signal.

10. The integrated circuit of claim 6, wherein the clock control logic comprises circuitry configured to enable the at least one clock signal in response to a bus grant signal.

11. The integrated circuit of claim 6, wherein the clock control logic comprises circuitry configured to enable the at least one clock signal substantially commensurate with a bus grant signal.

12. A method of assuming mastership of a bus comprising:

asserting a bus request signal;

disabling or inhibiting an internal clock signal substantially coincident with the bus request signal;

receiving a bus grant signal; and

enabling the internal clock signal substantially coincident with the bus grant signal.

13. The method of claim 12, wherein disabling the internal clock signal substantially coincident with the bus request signal comprises disabling the internal clock signal in response to an assertion of the bus request signal.

14. The method of claim 12, wherein disabling the internal clock signal substantially coincident with the bus request signal comprises disabling the internal clock signal after an assertion of the bus request signal.

15. The method of claim 12, wherein enabling the internal clock signal substantially coincident with the bus grant signal comprises enabling the internal clock signal in response to an assertion of the bus grant signal.

16. The method of claim 12, wherein enabling the internal clock signal substantially coincident with the bus grant signal comprises enabling the internal clock signal after an assertion of the bus grant signal.